CLAIMS:

1.   A data processor comprising one or more functional units, one or more register files, a data memory, and a snapshot buffer which during the handling of an interrupt condition accommodates to save state informations of various processor state elements in respective snapshot buffer elements,

5   said data processor being characterized by comprising controller means that are arranged for upon a subsequent interrupt condition that occurs during the handling of an actual interrupt condition saving the contents of said snapshot buffer elements in a data memory facility having a multibit access port facility.

10   2.   A data processor as claimed in Claim 1, wherein said controller means are arranged for upon completing the handling of an actual interrupt condition retrieving the earlier saved contents of said snapshot buffer elements from said data memory facility through said multibit access port facility back into said snapshot buffer elements.

15   3.   A data processor as claimed in Claim 2, wherein said controller means are arranged for upon said retrieving likewise restoring earlier saved state informations of various processor state elements allowing said data processor to proceed with handling an earlier uncompleted interrupt, or, as the case may be to proceed with continuing a main thread of the processing.

20

4.   A data processor as claimed in Claim 1, wherein said state informations comprise latency data of current operations.

5.   A data processor as claimed in Claim 1, wherein said snapshot buffer
25   comprises output multiplexer means having said multibit access port facility for sequentially saving selected snapshot buffer elements for transferring their contents to said data memory facility.

6.   A data processor as claimed in Claim 1, wherein said snapshot buffer comprises input multiplexer means having said multibit access port facility for sequentially selecting selected snapshot buffer elements for back-transferring their saved contents from said data memory facility.

7.   A data processor as claimed in Claim 1, wherein said data memory facility is operated as a stack.

8.   A data processor as claimed in Claim 7, wherein said stack has a stack pointer that allows multiple stack positions per snapshot.

9.   A data processor as claimed in claim 7, wherein write and read operations in said stack are executed at mutually exclusive instants in time.

10.   A data processor as claimed in Claim 1, wherein said snapshot buffer is at least substantially constructed from shadow flipflops for storing its snapshot information.

11.   A data processor as claimed in Claim 1, wherein said snapshot buffer is operated at low power through one or more of clocking shadow flipflops only during actual taking of a snapshot, which may imply activating the snapshot buffer during only one clock cycle, clocking only the shadow flipflops pointed to by the stack pointer as the top-of-stack-plus-one during a stack push operation, and clocking the stack pointer itself only during stack pointer updates that are caused by the popping and pushing, respectively, of the snapshot buffer stack.

12.   A data processor as claimed in Claim 1, having a plurality of parallel issue slots (32-38) of which only a single issue slot is used for implementing such handling of nested interrupts.

13.   A data processing facility comprising an embedded data processor as claimed in Claim 1.

14.   A method for operating a data processor as claimed in Claim 1 that is arranged for handling nested interrupts.